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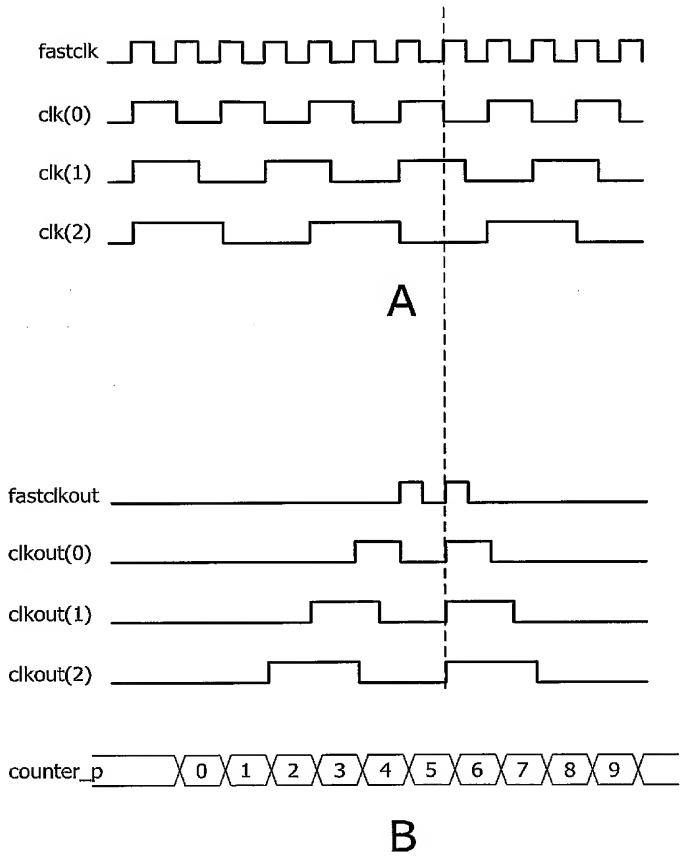
(54) Title: DELAY FAULT TEST CIRCUITRY AND RELATED METHOD



(57) Abstract: The invention provides for a delay fault test circuitry for producing a train of two clock pulses in response to two respective clock signals of different frequency associated with logic circuits to be tested and which are arranged to run at different speeds, and arranged such that the rising edges of the second of the clock pulses are aligned and further including counting means for producing a reference count value, means for initiating the first of the two clock pulses when the said count value reaches a first threshold value, means for ending the first of the two clock pulses when the said count value reaches a second threshold value, means for initiating the second of the two clock pulses when the said count value reaches a third threshold value; means for ending the second of the two clock pulses when the count value reaches a fourth threshold value, wherein the third threshold value is common for both input clock signals and the first, second and fourth threshold values are based on the respective frequencies of the clock signals.

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